REMARKS/ARGUMENTS

Favorable reconsideration and allowance of the present application are respectfully requested in view of the following remarks.

A. SUMMARY OF THIS AMENDMENT

By the current amendment, Applicant:

1. Amends claims 1-2, 5-6 and 8.
2. Respectfully traverses all prior art rejections.

This is in response to the Office Action dated April 14, 2009. Claims 1-6, 8, 10 and 11 are pending. Claims 1-6, 8, 10 and 11 stand rejected in the outstanding Office Action. Claims 1-2, 5-6 and 8 have been amended.

B. OBJECTION TO THE DRAWINGS

The objection to the drawings is respectfully traversed. The Examiner objected to the drawings, as allegedly not showing every claimed feature, e.g., "a thicker concave portion and thinner convex portion wherein each convex portion has the front electrode (as claimed in claim 5)", see section 7 on p. 7 of the Office Action of 4/14/2009. Claim 5 has been amended to recite "wherein each *concave* portion has the front electrode". Claim 5 depends from claim 4, which corresponds to Fig. 6 of the instant specification. As can be seen in Fig. 6, the concave portions have the surface electrodes 88.

C. OBJECTION TO THE SPECIFICATION

The objection to the specification is respectfully traversed. The Examiner objected to the specification as allegedly not supporting the limitation "forming a front electrode that is in partial direct physical contact with the convex portion which constitutes a part of the semiconductor substrate surface", recited in claim 6. The Examiner asserted that the original disclosure shows

that the front electrode is in partial direct contact with the second conductivity type semiconductor layer not with the convex portion which constitutes a part of the semiconductor substrate surface.

According to the specification (p. 20, line 6 to p. 21, line 3), during the fabrication of the device, the second conductivity type semiconductor layer is formed by thermally diffusing N-type impurities into the p-type (e.g., first conductivity type) semiconductor substrate, therefore, the N-type layer is part of the semiconductor substrate. Hence, the claim language "forming a front electrode that is in partial direct physical contact with the convex portion which constitutes a part of the semiconductor substrate surface" is supported by the disclosure.

Similarly, the Examiner objected to the specification as allegedly not supporting the limitation "forming a front electrode that is in partial direct physical contact with the concave portion which constitutes a part of the semiconductor substrate surface", recited in claim 8. The Examiner asserted that the original disclosure shows that the front electrode is in partial direct contact with the second conductivity type semiconductor layer not with the concave portion which constitutes a part of the semiconductor substrate surface.

As discussed above, the N-type layer is part of the p-type (e.g., first conductivity type) semiconductor substrate, since the N-type layer is formed by thermally diffusing the N-type impurities from the coating film into the p-type substrate (p. 27, line 14 to p. 28, line 7), hence the claim language has support in the specification.

D. PATENTABILITY OF THE CLAIMS

The rejection of claims 6 and 8 under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement, is respectfully traversed.

More specifically, the Examiner asserted that the limitations mentioned above (section B) do not have support in the specification. As explained above, the specification discloses a fabrication method where second conductivity type impurities are diffused into the first conductivity type semiconductor substrate, hence they become part of the substrate. Therefore, it is respectfully requested that the 112, first paragraph rejection be withdrawn.

The rejection of claims 5-6 and 8 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite, is respectfully traversed.

Claim 5 has been amended to recite "wherein each *concave* portion has the front electrode" to overcome the Examiner's rejection.

Finally, the Examiner also rejected claims 6 and 8, as allegedly being indefinite for containing the claim limitations mentioned above (section B). As explained above, the specification discloses a fabrication method where second conductivity type impurities are diffused into the first conductivity type semiconductor substrate, hence they become part of the substrate. Therefore, it is respectfully requested that the 112, second paragraph rejection be withdrawn.

The rejection of independent claim 1, as allegedly being anticipated under 35 U.S.C. § 102(b) by Nakai et al. (US 6,207,890) is respectfully traversed. Nakai fails to disclose or even remotely suggest each and every limitation set forth in the claim. Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", *Verdegaal Bro. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (MPEP § 2131).

The Examiner identified the intrinsic layer 2 as the claimed first conductivity type semiconductor substrate, and the p-type layer 3 as the claimed second conductivity type

semiconductor layer (see Fig. 1 in Nakai). Moreover, the Examiner asserted that layer 3 is being partially in direct physical contact with the front electrode 4 and becoming thinner as it goes farther from the contacted area "layer 3 becomes thickest at the peak, i.e., convex portion and thins out as it goes away from the peak", see section 14 on p. 7 of the Office Action of 4/14/2009.

First, layer 2 identified by the Examiner as the claimed substrate, is not a substrate. Nakai very clearly characterizes 1 as the substrate and 2 as a layer formed on the substrate "a problem may occur when the intrinsic amorphous silicon layer 2 is formed on the substrate 1 by a plasma CVD method", col. 1, lines 62-64. It is well known in the art that a substrate has completely different physical characteristics compared to a layer that is formed on the substrate.

Second, unlike the Examiner's assertion, the front electrode 4 is in full contact with layer 3, identified as the claimed second conductivity type semiconductor layer, as opposed to the claimed device where the front electrode is "being partially in direct physical contact" with the second conductivity type semiconductor layer. Even though layer 3 becomes thinner further away from the peak, Nakai does not teach or suggest that layer 3 seizes to be in full contact with the front electrode at any point.

The rejection of independent claims 1 and 8, as allegedly being anticipated under 35 U.S.C. § 102(b) by Okamoto et al. (JP 04-356972) is respectfully traversed. Okamoto fails to disclose or even remotely suggest each and every limitation set forth in the claims. Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", *Verdegaal Bro. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (MPEP § 2131).

Amended claims 1 and 8 now recite "wherein the second conductivity type semiconductor layer has the convex and concave portions along the convex and concave portions of the first conductivity type semiconductor substrate, respectively". Support for the amendment can be found, for example, in Fig. 1 of the instant specification. Okamoto fails to teach or suggest this limitation.

Okamoto discloses a photoelectric transducer (Fig. 1) comprising a first conductivity type (p-type) semiconductor substrate 10, a second conductivity type (N-type) semiconductor layer 1 formed on the surface of the substrate 10 and being in direct contact with the substrate 10, and a front electrode 5 being in partial direct physical contact with the N-type layer 1, wherein the N-type layer becomes thinner as it goes further from the contacted area.

As can be seen in Fig. 1 of Okamoto, the first conductivity type semiconductor substrate 10 and the second conductivity type semiconductor layer 1 are arranged in such a way that the convex portions of layer 1 are aligned with the concave portions of the substrate 10 and the concave portions of layer 1 are aligned with the convex portions of the substrate 10. This is exactly opposite to the configuration of claims 1 and 8 where the convex portions and the concave portions of the first and the second conductivity type layers are aligned.

In addition, regarding claim 8, Okamoto does not disclose "forming a film containing second conductivity type impurities on a semiconductor substrate having convex and concave portions formed on its surface in such a manner that the film becomes thicker from the convex portion to the concave portion; (b) implanting second conductivity type impurities into the semiconductor substrate from the film", as required by claim 8. In Okamoto, the p-type semiconductor substrate 10 is doped "by being irradiated with a laser, such as a 308 nm-wavelength XeCl excimer laser, in varying conditions inside a vapor phase that contained and n-

type dopant", see paragraph [0023]. In contrast, in the claimed device, first a coating solution containing N type impurities (such as PSG liquid) is applied by spin coating onto a P type semiconductor substrate, and then the coating film is dried and heated to diffuse the N type impurities from the coating film to the P type semiconductor substrate, thereby forming an N type semiconductor layer (p. 27, line 14 to p. 28, line 7 in the instant specification). This is not taught in Okamoto in fabricating the device of Fig. 1. Okamoto does not teach forming a film on the substrate to implant the N-type impurities.

The rejection of independent claim 6, as allegedly being anticipated under 35 U.S.C. § 102(b) by Nishitani et al. (US 6,023,020) is respectfully traversed. Nishitani fails to disclose or even remotely suggest each and every limitation set forth in the claim. Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", *Verdegaal Bro. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (MPEP § 2131).

The Examiner identified high-resistance film 7 as the claimed film serving as a barrier against diffusion into the semiconductor substrate (identified as the light absorbing layer 3), and window layer 4 as the source of implanting second conductivity type impurities into layer 3 through the film 7. Finally, the Examiner asserted that front electrode 5 is in contact with the convex portion (peak) which constitutes a part of the semiconductor substrate 3 and alleged that "the front electrode, as claimed, can not be in partial direct physical contact with the convex portion (see fig. 2) which constitutes a part of the semiconductor substrate surface, due to presence of an intervening layer-second conductivity type semiconductor layer", see section 16 on p. 11 of the Office Action of 4/14/2009.

First, forming a layer 4 onto the high-resistance film 6 does not imply that second type conductivity type impurities are implanted into the semiconductor substrate 3. In the claimed device, this step corresponds to heating the N-type film formed on the substrate to diffuse the N-type impurities from the film to the substrate. This step is absent from Nishitani.

Second, film 7 is formed in an island pattern at sections 12 on layer 3 (Fig. 2 in Nishitani). However, the "island" patterns 12 are not such that "the film becomes thicker from the convex portion to the concave portion", as required by claim 6. More specifically, the cited "convex portion" and "concave portion" in the claim language refer to portions of the "semiconductor substrate", e.g., layer 3. Thus, the convex portion corresponds to a peak and the concave portion corresponds to a trough. However, as can be seen in Fig. 2, there is no film 7 at the peak areas of layer 3, and in fact, the film 7 areas become thicker from the concave portion to the convex portion, not from the convex portion to the concave portion, as required by claim 6.

Finally, unlike the Examiner's assertion, front electrode 5 is not in partial contact with the convex portion which constitutes a part of the semiconductor substrate surface. The convex portion which constitutes a part of the semiconductor substrate surface is part of the layer 3. As can be seen from Fig. 2, electrode 5 is not even in contact with layer 3, as there is an intervening layer 4 between the electrode 5 and the semiconductor layer 3. In contrast, in the device made by the method of claim 6, the front electrode 8 is partially in direct physical contact with the convex portions of the substrate 4 which contain an n-type layer on the top part thereof (implanted via thermal diffusion), see Fig. 1 of the instant specification.

For the above reasons, claims 1, 6 and 8 are allowable.

It is respectfully requested that the rejection of claims 2-5 and 10-11, all dependent from claim 1, also be withdrawn.

E. MISCELLANEOUS

In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

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